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REMARKS

Prior to the present amendment and response, claims 1-7, 9-11, 13-21, and 32-34 were pending in the present application. By the present amendment, claim 1 has been amended and claim 2 has been canceled. Thus, after the present amendment, claims 1, 3-7, 9-11, 13-21, and 32-34 remain in the present application. Reconsideration and allowance of outstanding claims 1, 3-7, 9-11, 13-21, and 32-34 in view of the above amendments and the following remarks are respectfully requested.

A. Objection to Drawings

The Examiner has objected to the drawings of the present invention under 37 CFR 1.83(a) by stating that “[t]he drawings must show every feature of the invention specified in the claims” and that “the multiple stop bits that correspond to endings of issue groups and information corresponding to chaining (claim 1) must be shown or the feature(s) canceled from the claim(s).” Present office action, page 2.

Applicant, however, respectfully submits that under 35 U.S.C. 113, a drawing shall be furnished by the applicant “where necessary for the understanding of the subject matter to be patented.” Thus, in the present application, Figure 2 adequately illustrates the invention’s method for encoding a composite VLIW packet using a tree structure as shown in tree structure 200. Exemplary first level (i.e., node 204), second level (i.e., nodes 210 and 212), and third level (i.e., nodes 216, 218, 220) nodes have also

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been provided in tree structure 200 in Figure 2. Since many different combinations of branch levels and nodes are possible using the techniques disclosed in the present application, and since the same techniques disclosed can be used to encode all of these different combinations, they have not been shown to not obscure the invention. Thus, even if a drawing was necessary (and a drawing is not necessary in all cases), tree structure 200, coupled with the disclosure in the detailed description (see, for example, page 25, lines 10-18), does indeed show every feature of the invention specified in the claims as required by 37 CFR 1.83(a).

B. Rejection of Claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a) as being unpatentable over U.S. Patent Number 5,922,065 to Hull, et al. ("Hull") in view of U.S. Patent Number 6,457,173 to Gupta, et al. ("Gupta"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Hull and Gupta, either singly or in combination.

Various embodiments according to the present invention, as defined by amended independent claim 1, relate to decoding very long instruction word (VLIW) packets. Assembly code is provided for each one of a plurality of instructions in a first combination of instructions in a VLIW packet. A template is matched in the VLIW packet to a known template corresponding to one of a plurality of known syntaxes. The

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plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure and include programming notation that indicate the end of a particular issue group. Each of a plurality of second level nodes in the tree structure includes a combination of instruction types. A plurality of paths extends between node levels, and each node of the plurality of first level nodes and the plurality of second level nodes has a path to a node of a different node level. See, for example, Figure 2 of the present application.

In the present invention, once a resolved packet syntax is determined, the invention proceeds to match every term of the “resolved packet syntax” (for example, A_inst “;,” A_inst “;,” A_inst “++” “;,”) against the syntax associated with each of the 24 first level nodes, i.e. nodes 204, 206, and 208. See, for example, present application, page 26, lines 4-6. Each first level node is associated with a unique syntax. For example, first level node 204 is represented by the programming notation “MIsI” and the unique syntax associated with the programming notation “MIsI” is:

i1 “;,” i2 “;,” i3 “++” “;,”

When the resolved packet syntax (i.e. A_inst “;,” A_inst “;,” A_inst “++” “;,”) is compared to the syntax of node 204 (i.e. i1 “;,” i2 “;,” i3 “++” “;,”), the invention determines whether *every term* of the resolved packet syntax matches a corresponding term in the syntax of node 204 by looking for a “direct match” or an “indirect match” for the respective terms in the resolved packet syntax and the node syntax. See, for example, present application, page 26, lines 12-18. A direct match is when there is an identical

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match between a term in the resolved packet syntax and a corresponding term in the node syntax at branch level one (i.e. an identical match with a first level node). See, for example, present application, page 26, lines 18-20. An indirect match is when there is no identical match with a first level node, but there is an identical match between the term in the resolved packet syntax and the corresponding term in the node syntax at branch levels two, three, or a lower branch level. See, for example, present application, page 26, lines 20-22 and page 27, line 1.

For example, if the first term in the syntax of node 204 is “il” and the first term in the resolved packet syntax is “A_inst”, then it is apparent that the first term in the node syntax (i.e. “il”) is not identical to the first term in the resolved packet syntax (i.e. “A_inst”) and as such there is no direct match at branch level one. The invention then looks for an indirect match between the first term in the node syntax (i.e. “il”) and the first term in the resolved packet syntax (i.e. “A_inst”). To perform this determination, the invention attempts to determine the various instruction types that can be assigned to the term “il” at branch level two. As seen in Figure 2, each node at branch level two corresponds to a combination of various instructions. Examples of such instruction combinations are “MA”, “IA”, “ILX”, and “ALX”. For example, a node in branch level two corresponding to the instruction combination “MA” leads either to a type M instruction or to a type A instruction in branch level three. Thus, in the present example where the first term in the resolved packet syntax is “A_inst”, the invention will proceed

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to look for an indirect match (since no direct match was found at branch level two) in branch level three.

At branch level three, the invention finally determines a match between the node syntax term "i1" and the resolved packet syntax "A_inst". The reason is that node 218 at branch level three which corresponds to a type A instruction is identical with the resolved packet syntax "A_inst". Thus, the invention has verified that the first term in the syntax of node 204 (i.e. i1 ";;" i2 ";;" i3 "++" ";;") matches the first term in the resolved packet syntax (i.e. A_inst ";;" A_inst ";;" A_inst "++" ";;"). This match has been an indirect match since there was no match between the respective first terms of the node syntax and the resolved packet syntax at branch level one. Having matched the respective first terms in the node syntax and the resolved packet syntax, the invention will proceed to determine whether the remaining terms in the node syntax and the resolved packet syntax also match.

In contrast, Hull is directed to a processor that utilizes a template field for encoding a set of most useful instructions in a wide-word format. Hull, in table 40 of Figure 4, discloses various combinations of template field encoding and instruction slot mapping. However, Hull does not teach, disclose, or suggest "matching a template in said first composite packet to a known template corresponding to one of a plurality of known syntaxes that includes multiple stop bits that indicate an end of an issue group and provide chaining information, wherein said plurality of known syntaxes are arranged as a

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plurality of first level nodes in a tree structure...” as required by amended independent claim 1.

In contrast to the present invention as defined by amended independent claim 1, Gupta discloses a tree structure wherein root node 132 of the tree is the overall machine instruction. See, for example, Gupta, column 12, lines 14-15. Root node 132 represents a choice of instruction templates (see, for example, Gupta, column 12, lines 15-16), such that each of the templates “encode the sets of operations that issue concurrently.” Gupta, column 12, lines 22-23. Gupta further explains that “each template is partitioned into one or more operation issue slots.” Gupta, column 12, lines 26-27.

The next level of the tree in Gupta defines each of the concurrent issue slots, where “each slot is an OR node supporting a set of operation groups, called a super group (i.e., nodes 138, 140, 142), that are all mutually exclusive and have the same concurrency pattern.” Gupta, column 12, lines 39-43. Operation groups, such as operation group 143, lie below each super group where each operation group is an OR node that has a select field to choose among the various operation formats supported by operation group. See, for example, Gupta, column 12, lines 47-51.

Thus, Gupta does not teach, disclose, or suggest “matching each term in said one of said plurality of known syntaxes against a respective term in a resolved packet syntax using said tree structure” as required by amended independent claim 1. In fact, the encoding disclosed in Gupta teaches away from using matching techniques since “[e]ach template encodes the cross-product of the operations in each of its slots” based on the

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concurrency and exclusivity of the operations in an operation group. Gupta, column 13, lines 35-36. As such, Gupta also fails to teach, disclose, or suggest the novel use of “direct” and “indirect” matching of each respective term in the resolved packet syntax and the corresponding term in the node syntax to determine an appropriate template used to encode a VLIW packet, as disclosed in the present invention. Therefore, Gupta cannot be combined with Hull to achieve the present invention.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not taught, disclosed, or suggested by the art of record. Thus, amended independent claim 1 is patentably distinguishable over the art of record. As such, the claims depending from amended independent claim 1 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claim 1, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1, 3-7, 9-11, 13-21, and 32-34 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance Notice of Allowance directed to all claims 1, 3-7, 9-11, 13-21, and 32-34 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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